WHAT IS CLAIMED IS:

1. A semiconductor memory device selectively driving memory cells in accordance with an input signal inputted from an external part to output data or to input and output data, said semiconductor memory device comprising:

a memory cell array having dummy bit lines and bit lines adjacently disposed to each other, dummy memory cells different from each other being connected to said dummy bit lines respectively, and memory cells different from each other being connected to said bit lines respectively; and

a timing control circuit controlling a timing of a driving operation based on signals supplied via said dummy bit lines, when selectively driving the memory cell connected to said bit line.

2. The semiconductor memory device according to claim 1, wherein, in said memory cell array, said dummy bit lines are adjacently disposed at positions closer to said timing control circuit than an arbitrary one of said bit lines.

3. The semiconductor memory device according to claim 1, wherein, in said memory cell array, said dummy bit lines are adjacently disposed at positions more distant from said timing control circuit than an arbitrary one of said bit lines.

4. The semiconductor memory device according to claim 1, wherein, in said memory cell array, said

dummy bit lines are adjacently disposed and said bit lines are disposed on both sides of said dummy bit lines adjacently disposed.

5. The semiconductor memory device according to claim 1, wherein, in said memory cell array, said dummy bit lines are divided into two sets, and the dummy bit lines in one of the sets are adjacently disposed at a position closer to said timing control circuit than an arbitrary one of the bit lines and the dummy bit lines in the other set are adjacently disposed at a position more distant from said timing control circuit than an arbitrary one of the bit lines.

6. The semiconductor memory device according to claim 5, wherein said dummy bit lines are divided into two sets, one set consisting of N pieces (N is a natural number) of the dummy bit lines and the other set consisting of N pieces or (N + 1) pieces of the dummy bit lines.

7. The semiconductor memory device according to claim 1, wherein, in said memory cell array, said dummy bit lines are disposed at a predetermined pitch.

8. The semiconductor memory device according to claim 1, wherein, in said memory cell array, said dummy bit lines are divided into a plurality of sets each consisting of a substantially equal number of dummy bit lines, the dummy bit lines in each of the sets being adjacently disposed, and the plural sets

of the dummy bit lines being disposed at a predetermined pitch.

9. The semiconductor memory device according to claim 1, wherein said memory cell array is provided in plurality.

10. The semiconductor memory device according to claim 1, wherein said dummy bit lines are connected in series.

11. The semiconductor memory device according to claim 1, wherein said timing control circuit controls the timing of the driving operation based on a signal supplied via a dummy bit line with the slowest signal change among said dummy bit lines.

12. The semiconductor memory device according to claim 10, wherein said timing control circuit generates a timing generating signal based on the signals supplied via said dummy bit lines and controls the timing of the driving operation based on the generated timing generating signal.

13. The semiconductor memory device according to claim 1, wherein said timing control circuit has a logical arithmetic circuit having an input terminal to which each one end of said dummy bit lines are connected, and said logical arithmetic circuit inverts a signal level of an output signal in accordance with a change in the signals supplied via said dummy bit lines.

14. The semiconductor memory device according to claim 1, wherein said timing control circuit controls the timing of the driving operation based on a potential difference between a potential of said dummy bit lines and a reference potential.

15. The semiconductor memory device according to claim 1, wherein each of said dummy memory cells and said memory cells has two inverter circuits, said two inverter circuits have input terminals and output terminals mutually cross-coupled, and the input terminals of the two inverter circuits in each of the dummy memory cells are further connected to power sources supplying predetermined voltages.

16. The semiconductor memory device according to claim 1, wherein each of the dummy memory cells and the memory cells has two inverter circuits, the two inverter circuits in each of the memory cells have input terminals and output terminals mutually cross-coupled, and the two inverter circuits in each of the dummy memory cells have input terminals connected to power sources supplying predetermined voltages respectively and output terminals connected to different dummy bit lines respectively.

17. The semiconductor memory device according to claim 1, wherein a predetermined number of dummy memory cells are selectively driven among said dummy memory cells connected to said dummy bit lines respectively, the dummy memory cells being selected

in descending order of a distance in said dummy bit lines from said timing control circuit.

18. The semiconductor memory device according to claim 1, wherein said dummy bit lines are a plurality of dummy bit line pairs each consisting of two dummy bit lines, and said bit lines are bit line pairs each consisting of two bit lines.

19. The semiconductor memory device according to claim 18, wherein said timing control circuit controls the timing of the driving operation based on a signal supplied via one of said dummy bit lines in said dummy bit line pair.

20. The semiconductor memory device according to claim 1, wherein said memory cell array has a dummy word line for selectively driving a dummy memory cell connected to said dummy bit lines and a word line for selectively driving a memory cell connected to said bit lines.